IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Akhil K. Garlapati		
Title:	VOLTAGE REFERENCE GENERATOR CIRCUIT USING LOW-BETA EFFECT OF A CMOS BIPOLAR TRANSISTOR		
Application No.:	10/813,837	Filed:	March 31, 2004
Examiner:	Rajnikant B. Patel	Group Art Unit:	2838
Atty. Docket No.:	026-0044	Confirmation No.:	6047

September 18, 2006

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Commissioner for Patents
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RESPONSE AFTER FINAL REJECTION (37 C.F.R. § 1.116)

This paper is being submitted following the Final Rejection mailed on July 17, 2006. Since the two month period from the final rejection falls on a Sunday, the time for replying within the two month period is extended until Monday, September 18, 2006. In light of the Remarks herein, further examination is requested.

Any fees required by this paper are being provided as directed in an electronic submission of this paper or in a transmittal letter accompanying this paper. However, the Commissioner is hereby authorized to charge any deficiency in fees required by this paper and any additional fees under 37 C.F.R. § 1.16 or 1.17 which may be required during the pendency of this application, and to similarly credit any overpayment, to Deposit Account 50-0631.